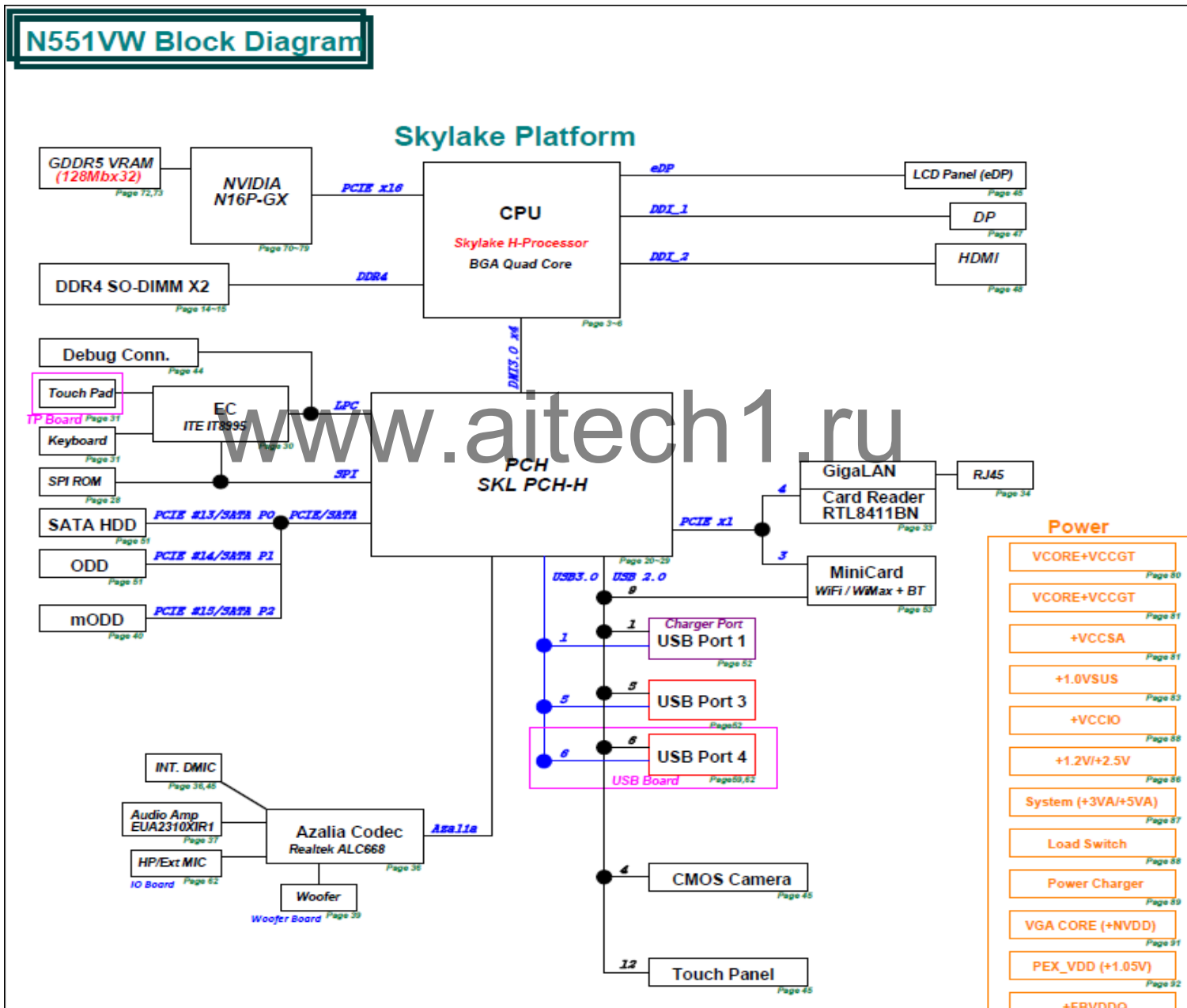
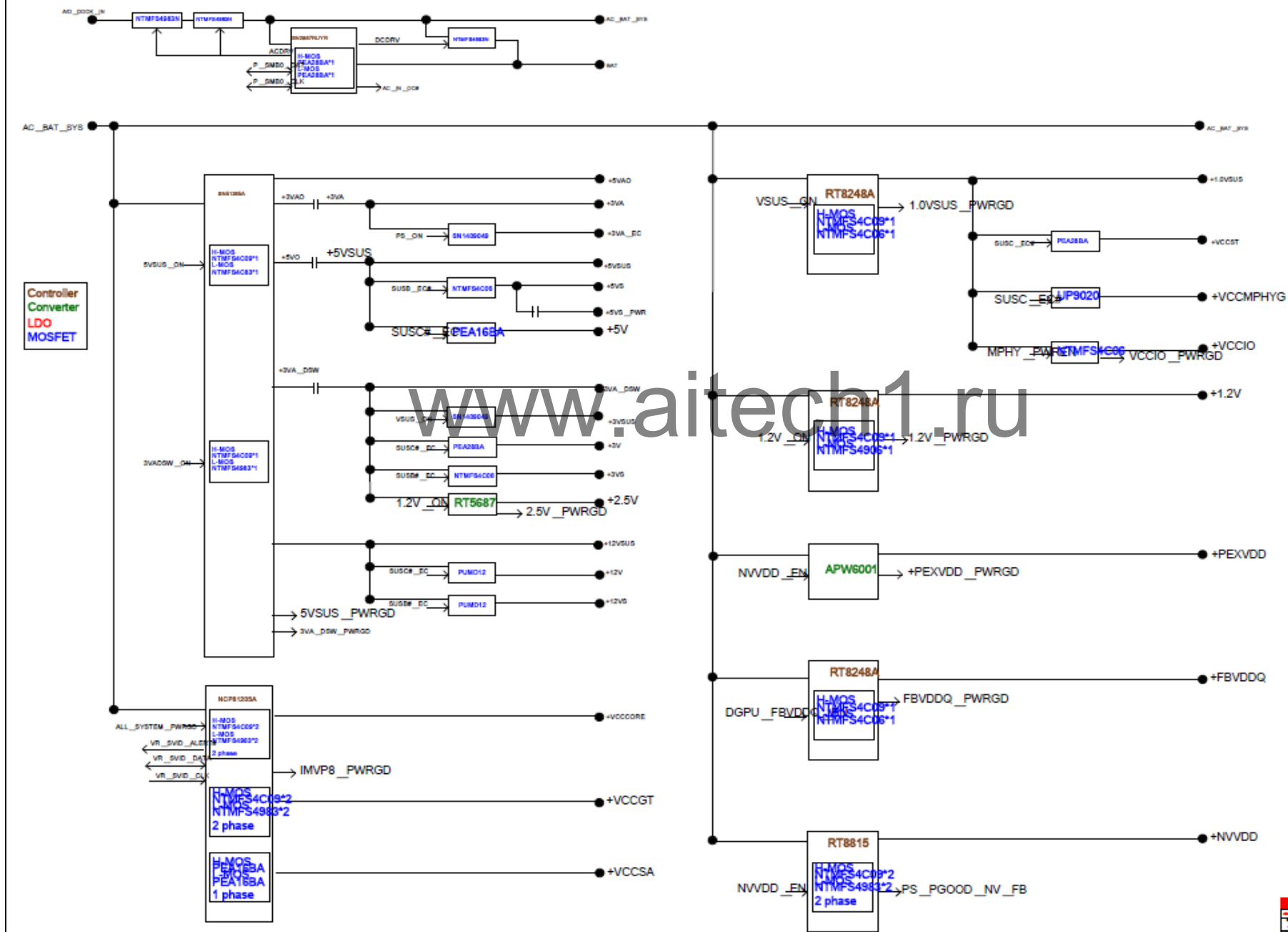


## BLOCK DIAGRAM

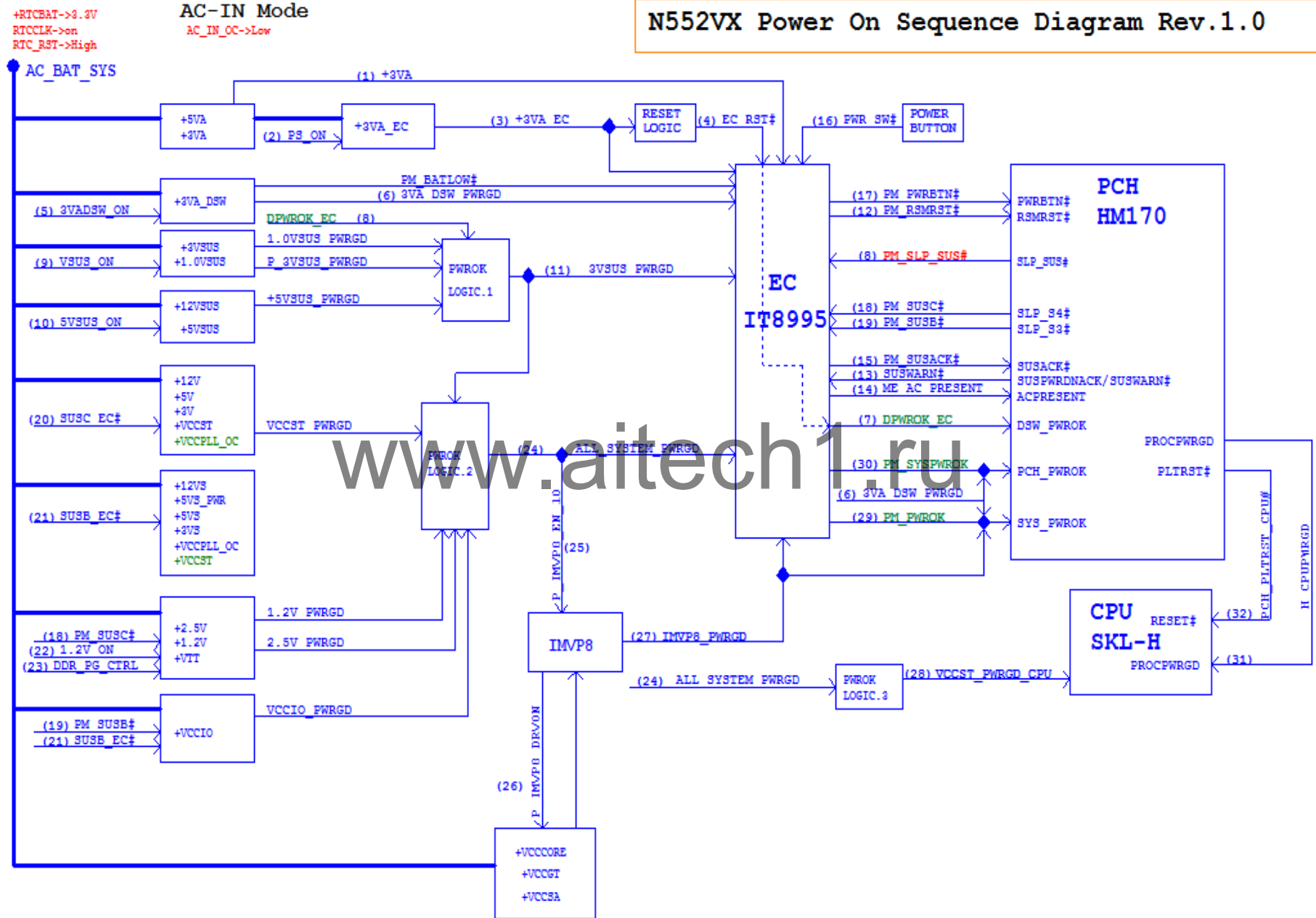


# POWER FLOW



# POWER ON SEQUENCE

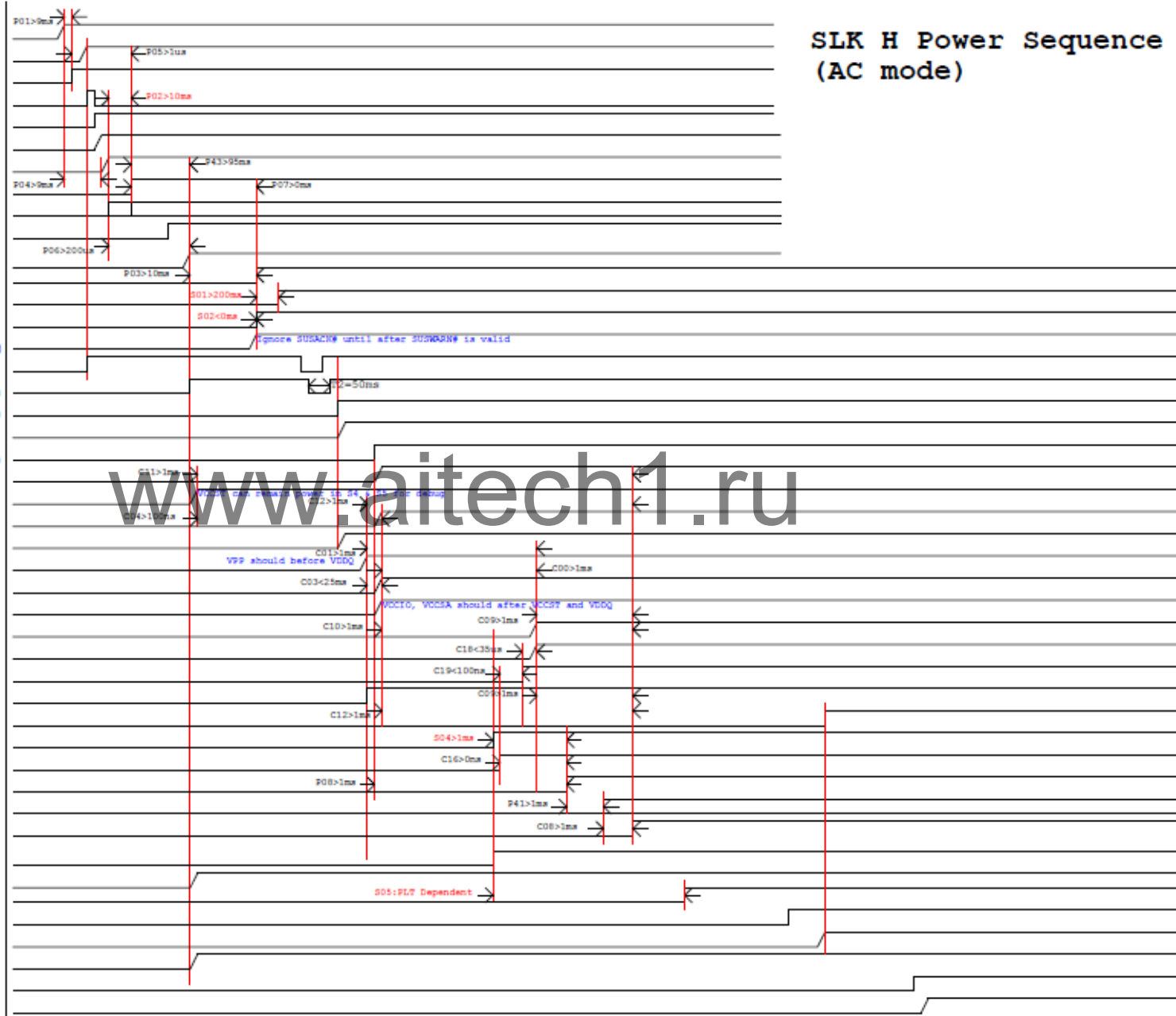
N552VX Power On Sequence Diagram Rev.1.0



# AC\_IN POWER ON SEQUENCE

## AC-IN Mode

C:CPU (+RTCBAT)+3VA\_RTC  
 P:PCH (AC\_BAT\_SYS)+3VA/+5VA  
 S:PLT (+3VA\_RTC) RTCRST# (PCH)  
 Power (Power) AC\_IN\_OC# (EC)  
 Signal (EC) PS\_ON (+3VA\_EC)  
 (PS\_ON)+3VA\_EC (EC)  
 (3VADSW\_ON)+3VA\_DSW (3VA\_DSW\_PWRGD)  
 (EC) DFWROK\_EC (PCH)  
 (+3VA\_DSW) PM\_BATLOW# (PCH)  
 (PCH) PM\_SLP\_SUS# (EC)  
 (VSUS\_ON)+1.0VSUS\_VCCPRIM (1.0VSUS\_PWRGD)  
 (EC) PM\_RSMRST#\_PCH (PCH)  
 (PCH) SUSWRN# (EC)  
 (EC) ME\_AC\_PRESENT\_PCH (PCH)  
 (EC) PCH\_SUSACK# (PCH)  
 (PWR\_Switch) PWR\_SW# (EC)  
 (EC) PM\_PWRBTN# (PCH)  
 (EC) SUSC\_EC# (Power)  
 (SUSC\_EC#)+12V/+5V/+3V  
 (EC) SUBS\_EC# (Power)  
 (SUBS\_EC#)+12VS/+5VS/+3VS  
 (VSUS\_ON)+1.0V\_VCCST,VCCPLL (VCCST\_PWRGD)  
 (+VCCIO)+VCCSTG  
 (1.2V\_ON)+2.5V (2.5V\_PWRGD)  
 (1.2V\_ON)+VDDQ\_CPU (1.2V\_PWRGD)  
 (+12VS)+VCCPLL\_OC  
 (SUBS\_EC#)+VCCIO (VCCIO\_PWRGD)  
 (ALL\_SYSTEM\_PWRGD)+VCCSA (IMVP8\_PWRGD)  
 (DDR\_VTT\_CTRL)+0.6V  
 (CPU) DDR\_VTT\_CTRL (Power)  
 (Power) 1.2V\_PWRGD (AND)  
 (Power) IMVP8\_PWRGD  
 (AND) ALL\_SYSTEM\_PWRGD (CPU/PCH/EC/Power)  
 (ALL\_SYSTEM\_PWRGD) VCCST\_PWRGD\_CPU (CPU)  
 (EC) PM\_PWRROK\_PCH (PCH)  
 (PCH) CLK\_PCH\_BCLK (CPU)  
 (PCH) H\_CPU\_PWRGD (CPU)  
 (ALL\_SYSTEM\_PWRGD) P\_IMVP8\_EN\_10 (Power)  
 (CPU) P\_SVID\_DATA\_X2 (Power)  
 (EC) PM\_SYSPWRROK\_PCH (PCH)  
 (PCH) PLT\_RST# (CPU/EC/Device)  
 (P\_IMVP8\_DRVON)+VCCCORE (IMVP8\_PWRGD)  
 (CPU) H\_THERMTRIP# (PCH)  
 (PCH) DDR4\_DRAMRST# (Memory)  
 +VCCGT



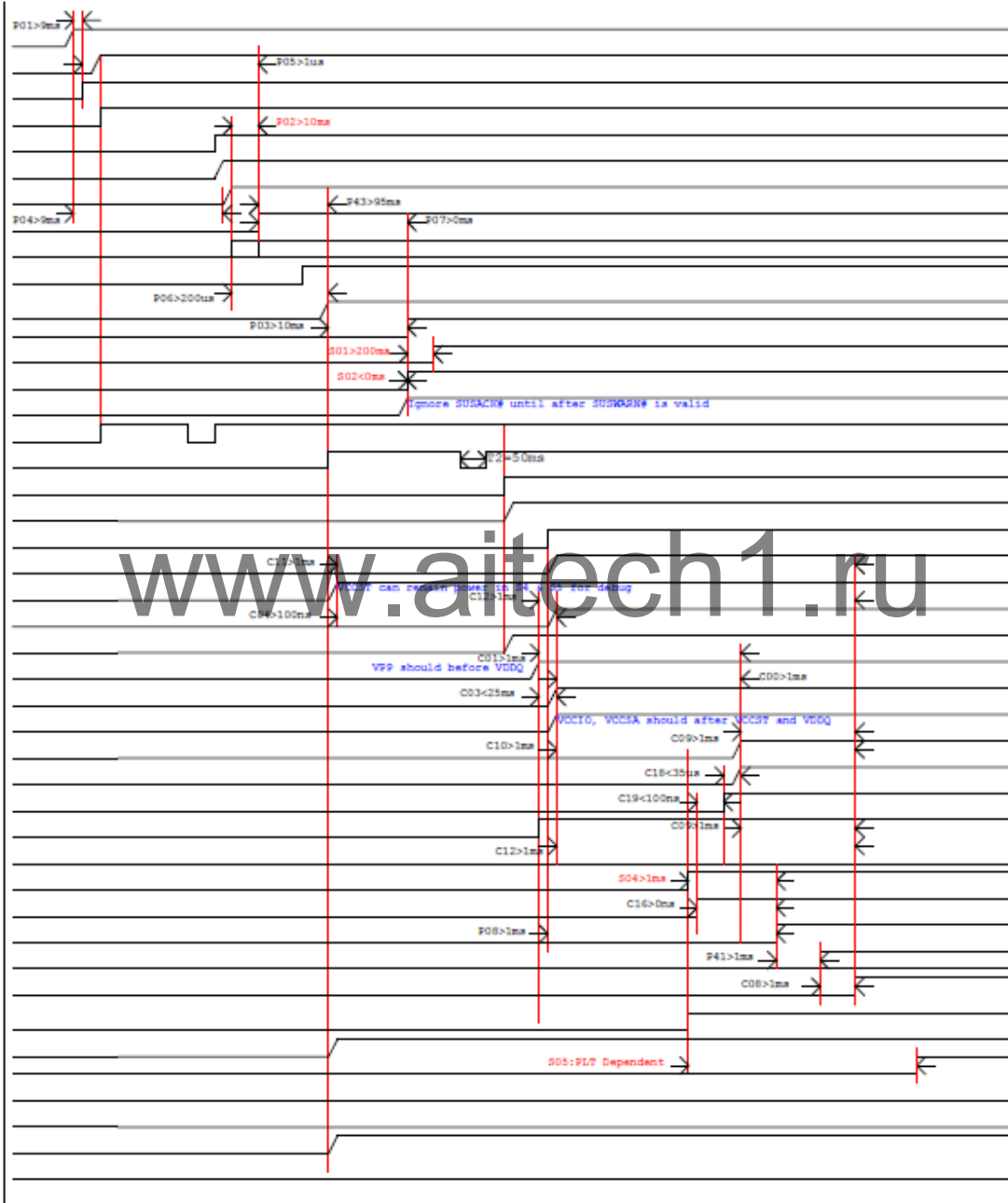
## SLK H Power Sequence (AC mode)

# DC\_IN POWER ON SEQUENCE

## DC-IN Mode

C: CPU  
 P: PCH  
 S: PLT  
 Power  
 Signal

(+RTCBAT) +3VA\_RTC  
 (AC\_BAT\_SYS) +3VA/+5VA  
 (+3VA\_RTC) RTCRST# (PCH)  
 (Power) AC\_IN\_OC# (EC)  
 (EC) PS\_ON (+3VA\_EC)  
 (PS\_ON) +3VA\_EC (EC)  
 (3VADSW\_ON) +3VA\_DSW (3VA\_DSW\_PWRGD)  
 (EC) DPWR0K\_EC (PCH)  
 (+3VA\_DSW) PM\_BATLOW# (PCH)  
 (PCH) PM\_SLP\_SUS# (EC)  
 (VSUS\_ON) +1.0VSUS\_VCCPRIM (1.0VSUS\_PWRGD)  
 (EC) PM\_RSMRST#\_PCH (PCH)  
 (PCH) SUSWARN# (EC)  
 (EC) ME\_AC\_PRESENT\_PCH (PCH)  
 (EC) PCH\_SUSACK# (PCH)  
 (PWR\_Switch) PWR\_SW# (EC)  
 (EC) PM\_PWRBTN# (PCH)  
 (EC) SUSC\_EC# (Power)  
 (SUSC\_EC#) +12V/+5V/+3V  
 (EC) SUSB\_EC# (Power)  
 (SUSB\_EC#) +12VS/+5VS/+3VS  
 (VSUS\_ON) +1.0V\_VCCST,VCCPLL (VCCST\_PWRGD)  
 (+VCCIO) +VCCSTG  
 (1.2V\_ON) +2.5V (2.5V\_PWRGD)  
 (1.2V\_ON) +VDDQ\_CPU (1.2V\_PWRGD)  
 (+12VS) +VCCPLL\_OC  
 (SUSB\_EC#) +VCCIO (VCCIO\_PWRGD)  
 (ALL\_SYSTEM\_PWRGD) +VCCSA (IMVP8\_PWRGD)  
 (DDR\_VTT\_CTRL) +0.6V  
 (CPU) DDR\_VTT\_CTRL (Power)  
 (Power) 1.2V\_PWRGD (AND)  
 (Power) IMVP8\_PWRGD  
 (AND) ALL\_SYSTEM\_PWRGD (CPU/PCH/EC/Power)  
 (ALL\_SYSTEM\_PWRGD) VCCST\_PWRGD\_CPU (CPU)  
 (EC) PM\_PWR0K\_PCH (PCH)  
 (PCH) CLK\_PCH\_BCLK (CPU)  
 (PCH) H\_CPU\_PWRGD (CPU)  
 (ALL\_SYSTEM\_PWRGD) P\_IMVP8\_EN\_10 (Power)  
 (CPU) P\_SVID\_DATA\_X2 (Power)  
 (EC) PM\_SYSFWR0K\_PCH (PCH)  
 (PCH) PLT\_RST# (CPU/EC/Device)  
 (P\_IMVP8\_DRVON) +VCCCORE (IMVP8\_PWRGD)  
 (CPU) H\_THERMTRIP# (PCH)  
 (PCH) DDR4\_DRAMRST# (Memory)  
 +VCCGT

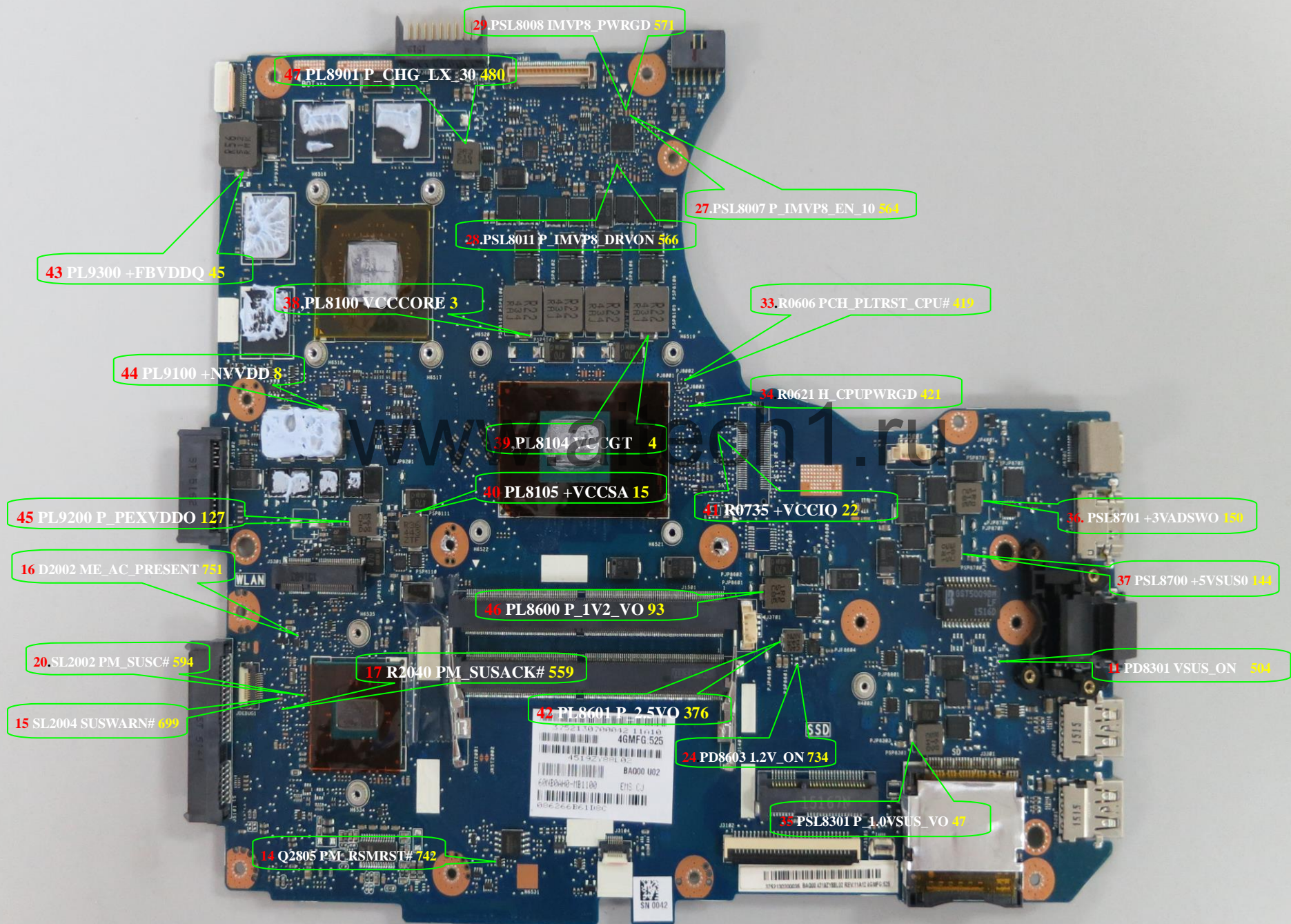


## SLK H Power Sequence (DC mode)

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## Signal Measure Point-Bottom





# Signal Measure Point-Top

